DisplayModule

DM-OLED069-642

0.69” 96 X 16 MONOCHROME GRAPHIC OLED DISPLAY MODULE - I2C

Contents

1 Revision History

Date	Changes
2019-03-06	First release
2020-03-13	Second release

2 Main Features

Item	Specification	Unit
Diagonal Size	0.69	inch
Display Mode	Passive Matrix OLED	-
Display Colors	Monochrome White	Colors
Resolution	96 x 16	pixel
Controller IC	SSD1306	-
Duty	1/16	duty
Interface	I2C	-
Active Area	17.26 x 3.18	mm
Module Dimension	32.54 x 10.0 x 2.7	mm
Weight	TBD	g

3 Pin Description

3.1 Panel Pin Description

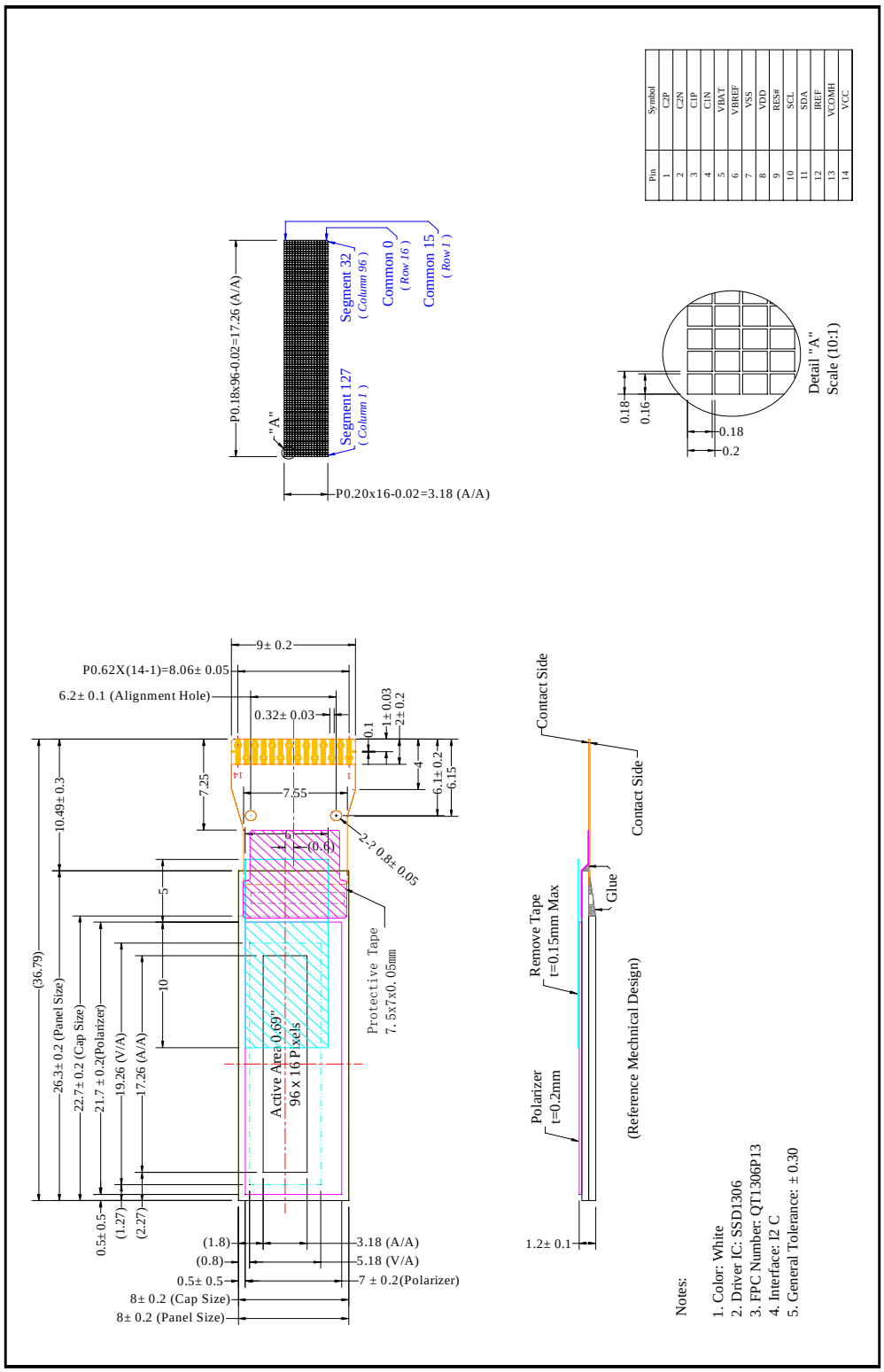
Pin No.	Symbol	Function Description
1-2 3-4	C2P/C2N C1P/C1N	Negative Terminal of the Flying Boost Capacitor Positive Terminal of the Flying Inverting Capacitor The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.
5	VBAT	Power Supply for DC/DC Converter Circuit This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to VDD when the converter is not used.
6	VBREF	NC
7	VSS	Ground of Logic Circuit This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.
8	VDD	Power Supply for Logic This is a voltage supply pin. It must be connected to external source.
9	RES#	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
10	SCL	IIC Bus Clock Signal The transmission if information in the I2C bus is following a clock signal .Each transmission of data bit is taken place during a single clock period of this pin.
11	SDA	IIC Bus Date Signal This pin acts as a communication channel between the transmitter and the receiver.
12	RES#	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
13	VCOMH	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
14	VCC	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used.

3.2 Module Pin Description

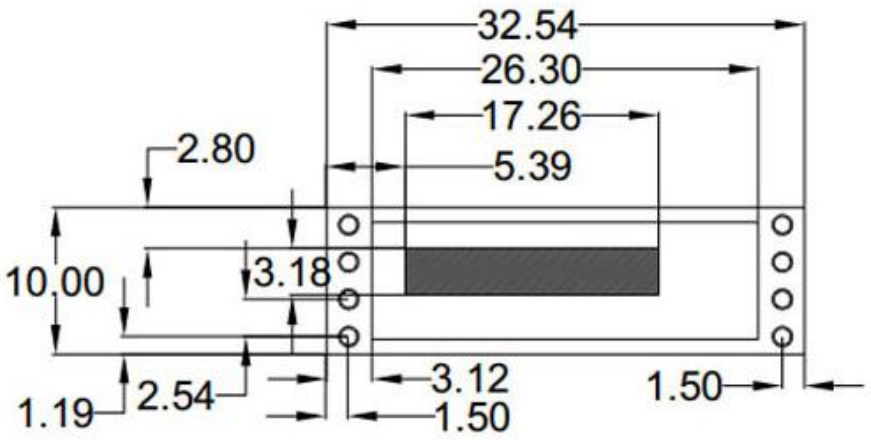
Pin No.	Symbol	Function Description
1	GND	Ground
2	VCC	Power Supply (3.3~5V)
3	SCL	IIC Clock
4	SDA	IIC Date

4 Mechanical Drawing

4.1 Panel Mechanical Drawing



4.2 Module Mechanical Drawing



5 Electrical Characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage for Logic	VDD		1.65	2.8	3.3	V
Supply Voltage for DC/DC	V_{BAT}	Internal DC/DC Enable	3.3	-	4.2	V
Supply Voltage for Display (Generated by Internal DC/DC)	VCC	Internal DC/DC Enable	7.0	-	7.25	V
Operating Current	ICC	Note 1	-	10	15	mA
Low Level Input Voltage	V_{IL}		0	-	$0.2xV_{DD}$	V
High Level Input Voltage	V_{IH}		$0.8xV_{DD}$	-	V_{DD}	V
Low Level Output Voltage	V_{OL}		0		$0.1xV_{DD}$	V
High Level Output Voltage	V_{OH}		$0.9xV_{DD}$		V_{DD}	V
Operating Temperature	TOP	Absolute Max	-40		85	°C
Storage Temperature	TST	Absolute Max	-40		85	°C

Note 1: VDD = 2.8V, VCC = 7.25V, 100% Display Area Turn on.

6 Optical Characteristics

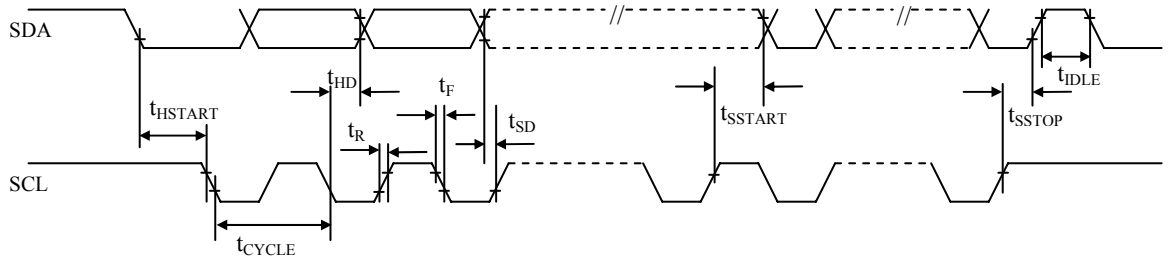
Item	Symbol	Min	Typ	Max	Unit
View Angles			Free		°
Response Time (25°C)	Tr + Tf				us
Brightness		120	150	-	cd/m^2
Contrast Ratio	CR		2,000:1		
Lifetime		10,000			Hrs

7 Timing Characteristics

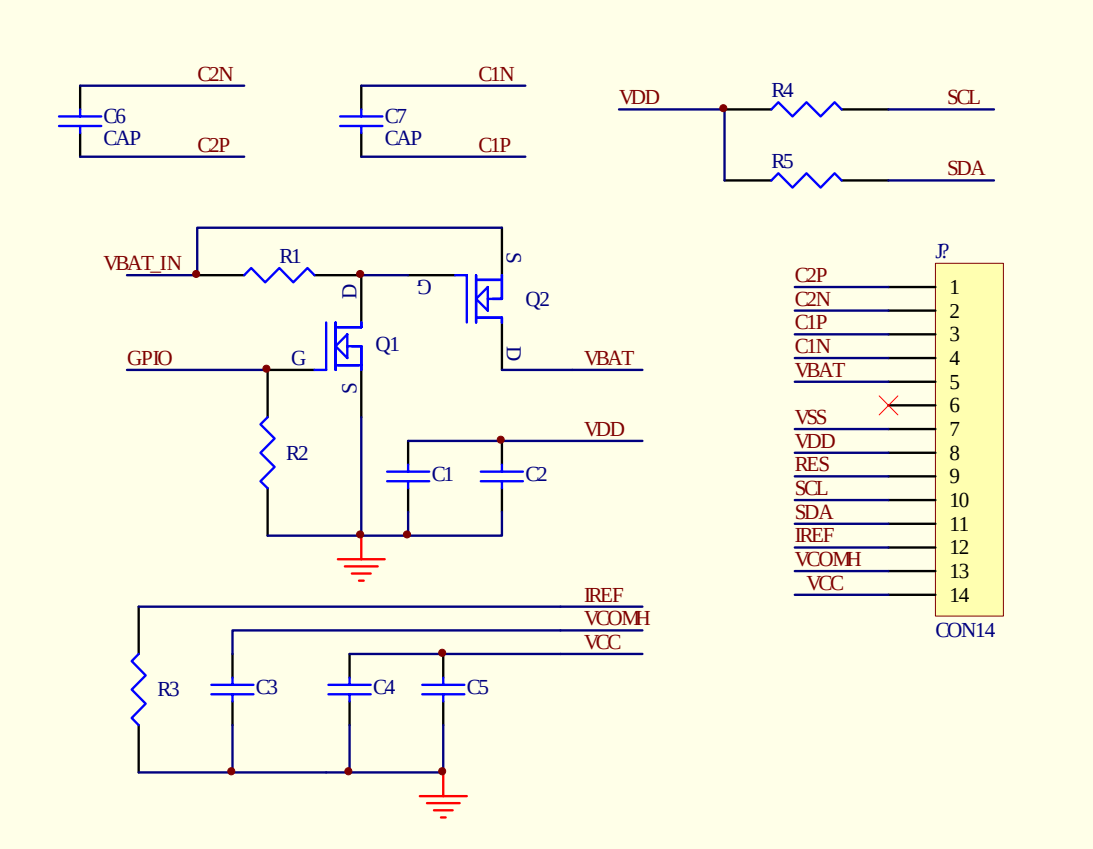
7.1 I2C Interface Timing Characteristics

TA=25℃,VDD-VSS=1.65-3.5V

Symbol	Item	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	µs
t_{HSTART}	Start Condition Hold Time	0.6	-	-	µs
t_{HD}	Data Hold Time (for "SDA_{OUT}" Pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" Pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start Condition)	0.6	-	-	µs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	-	µs
t_R	Rise Time for Data and Clock Pin	-	-	300	ns
t_F	Fall Time for Data and Clock Pin	-	-	300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	-	µs



7.2 I2C Interface With Internal Charge Pump



Recommended Components:

C1,: 0.1 μ F / 6.3V, X5R

C2: 4.7 μ F / 6.3V, X5R

C3: 2.2 μ F/ 16V, X7R

C4: 4.7 μ F / 16V, X7R

C5: 0.1 μ F / 16V, X7R

C6,C7: 1 μ F / 16V, X7R

R3: 560KΩ, R3 = (Voltage at IREF - VSS) / IREF

R2, R1: 47kΩ

R4, R5: 4.7kΩ

Q1: FDN338P

Q2: FDN335N

Notes:

VDD: 1.65~3.3V, it should be equal to MPU I/O voltage.

VBAT_in: 3.5~4.2V

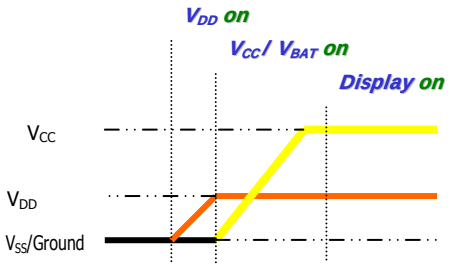
8 Functional Specification

8.1 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

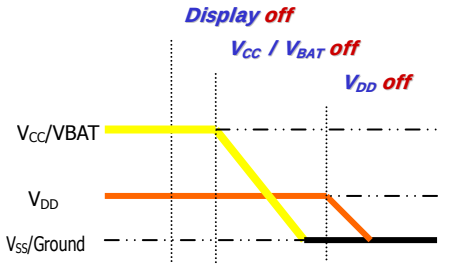
Power up Sequence

1. Power up V_{DD}/V_{BAT}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms(When V_{CC} is stable)
7. Send Display on command



Power down Sequence

1. Send Display off command
2. Power down V_{CC}/V_{BAT}
3. Delay 100ms
   (When V_{CC}/V_{BAT} is reach 0 and panel is completely discharges)
4. Power down V_{DD}

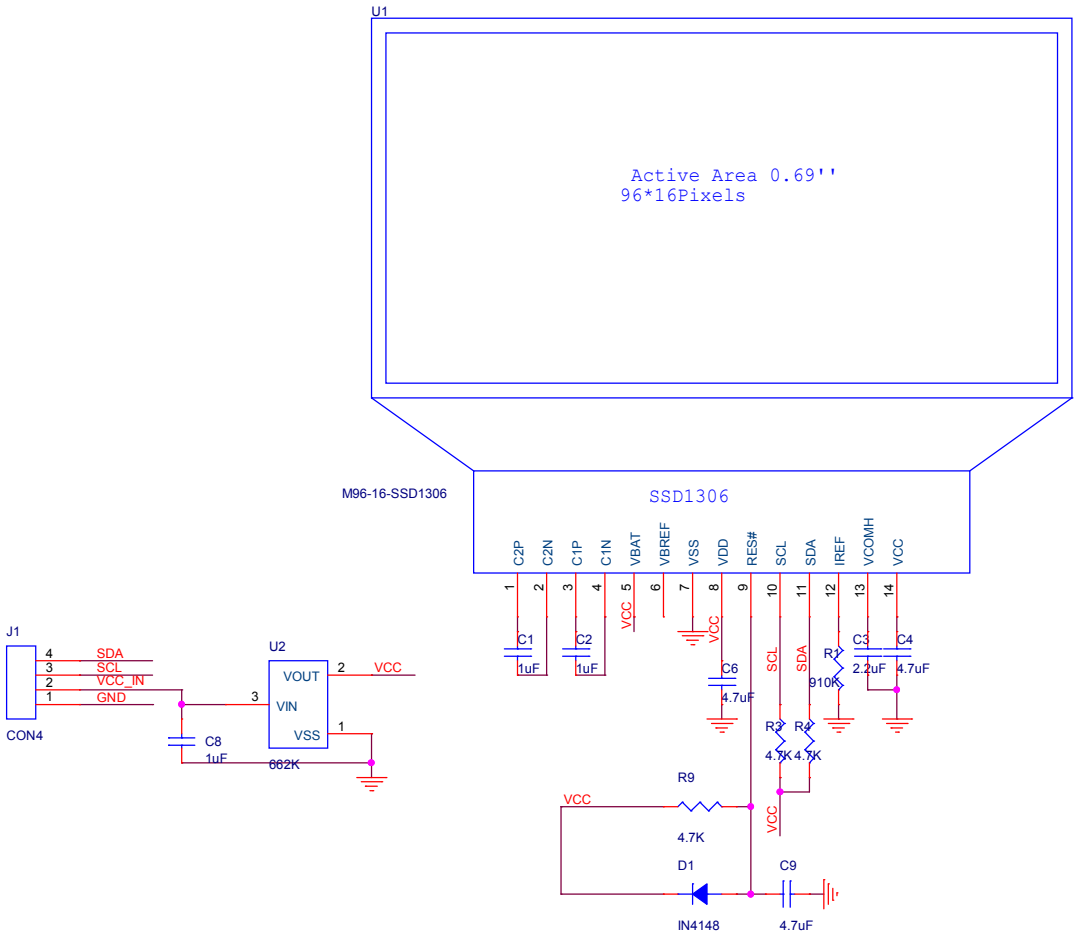


8.2 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128x32 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

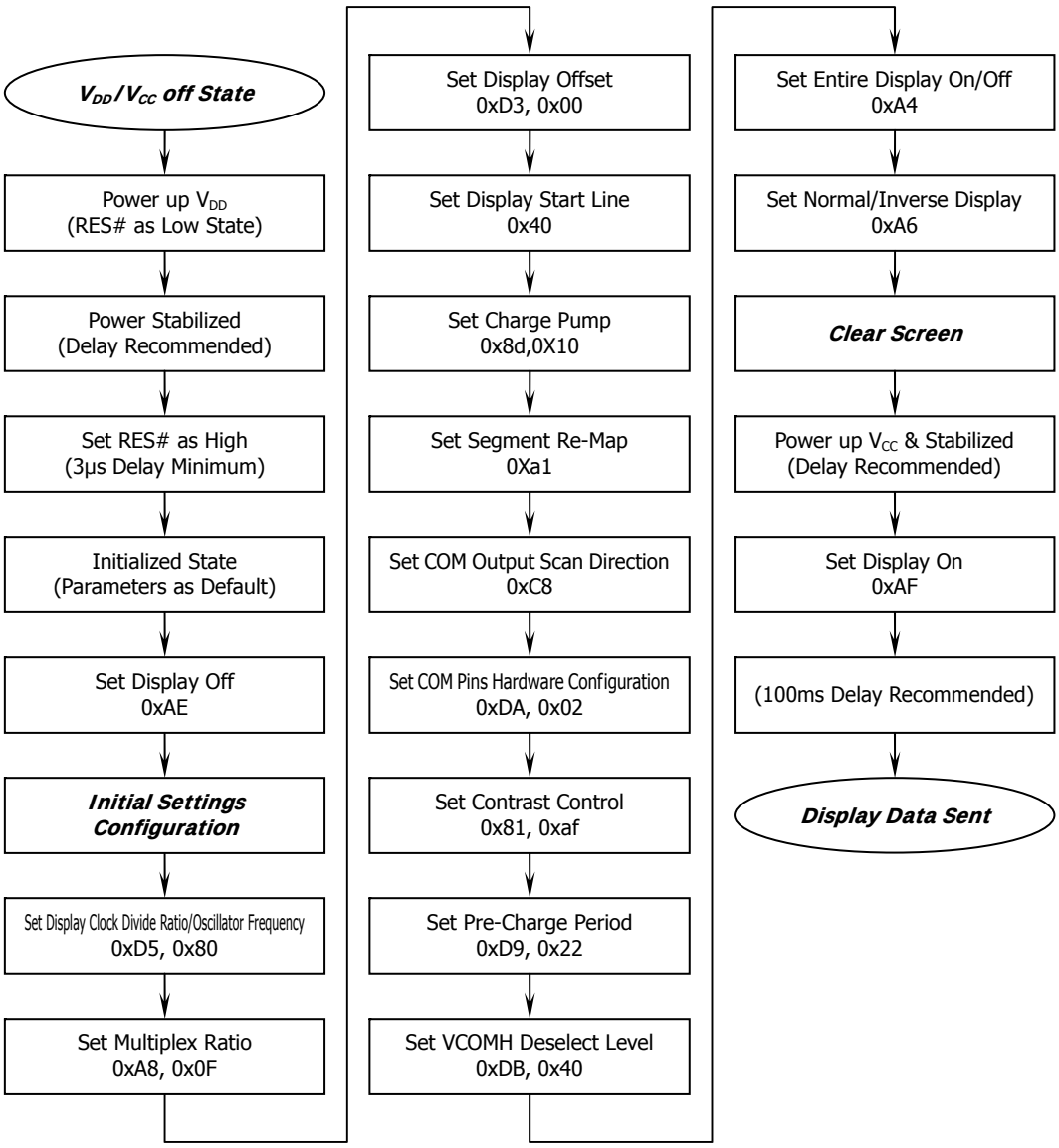
9 Module Schematic



10 Example Application

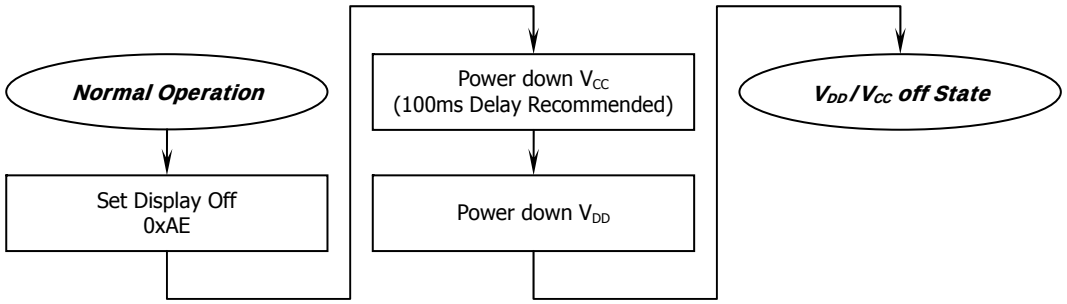
VCC Generated by Internal DC/DC Circuit

<Power up Sequence>

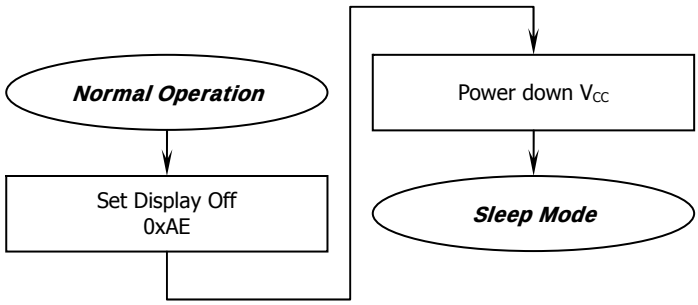


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

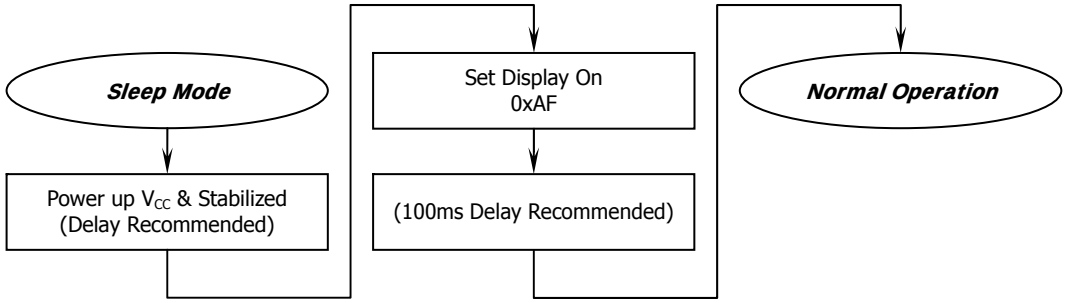
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



Internal setting（Charge pump）

```
void sh1106()
{
 RES=0;
 delay(1000);
 RES=1;
 delay(1000);
  write_i(0xAE); /*display off*/
  write_i(0x00); /*set lower column address*/
   write_i(0x10); /*set higher column address*/
  write_i(0x40); /*set display start line*/
  write_i(0xb0); /*set page address*/
  write_i(0x81); /*contract control*/
```

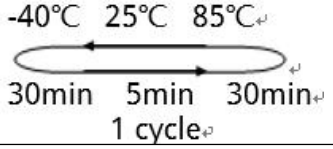
```
write_i(0xAF); /*128*/
 write_i(0xA1); /*set segment remap*/
 write_i(0xA6); /*normal / reverse*/
 write_i(0xA8); /*multiplex ratio*/
write_i(0x0F); /*duty = 1/16*/
write_i(0xC8); /*Com scan direction*/
 write_i(0xD3); /*set display offset*/
 write_i(0x00);
  write_i(0xD5); /*set osc division*/
 write_i(0x80);
  write_i(0xD9); /*set pre-charge period*/
 write_i(0x22);
  write_i(0xDA); /*set COM pins*/
 write_i(0x02);
  write_i(0xdb); /*set vcomh*/
 write_i(0x40);
  write_i(0x8d); /*set charge pump enable*/
 write_i(0x14);
  write_i(0xAF); /*display ON*/
  }

void write_w(unsigned char dat)
{
 unsigned char m,da;
 unsigned char j;
 da=dat;
 for(j=0;j<8;j++)
 {
 m=da;
 SCL=0;
 m=m&0x80;
if(m==0x80)
 {
 SDA=1;
 }
 else
 {
 SDA=0;
 }
 da=da<<1;
 SCL=1;
 }
 SCL=0;
 SCL=1;
}
```

```
void write_i(unsigned char ins)
{
 start();
 write_w(0x78);
 write_w(0x00);
 write_w(ins);
 stop();
}

void write_d(unsigned char dat)
{
 start();
 write_w(0x78);
 write_w(0x40);
 write_w(dat);
 stop();
}


 void start()
{
 SCL=1;
 SDA=1;
 SDA=0;
 SCL=0;
}

void stop()
{
 SCL=0;
 SDA=0;
 SDA=1;
 SCL=1;
}

void delay(unsigned int t)
{
 while(t>0)
 {
 t--;
 }
}
```

11 Command Table

Please check Driver IC datasheet

12 Reliability

Test Item	Content of Test	Test Condition	Note
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	85°C 200hrs	2
Low Temperature Storage	Endurance test applying the high storage temperature for a long time.	-40°C 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	85°C 200hrs	-
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-40 °C 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60°C,90%RH max, for 96hrs under no-load condition excluding the polarizer. Then taking it out and drying it at normal temperature.	60°C,90%RH 96hrs	1,2
Thermal Shock Resistance	The sample should be allowed stand the following 10 cycles of operation 	-40°C/85°C 10 cycles	-
Vibration Test	Endurance test applying the vibration during transportation and using	Total fixed amplitude: 15mm; Vibration: 10~55Hz; One cycle 60 seconds to 3 directions of X, Y, Z, for each 16 minutes.	3
Static Electricity Test	Endurance test apply the electric stress to the terminal.	VS=800V, RS=1.5kΩ, CS=100pF, 1 time.	-

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal. Temperature and humidity after remove from the rest chamber.

Note3: Test performed on product itself, not inside a container.

13 Warranty and Conditions

http://www.displaymodule.com/pages/faq HYPERLINK "http://www.displaymodule.com/pages/faq"